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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/785,604	02/16/2001	Hyun Lee	14-5-3	4376

7590 01/26/2004

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EXAMINER

DU, THUAN N

ART UNIT	PAPER NUMBER
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2116

DATE MAILED: 01/26/2004

6

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/785,604

Applicant(s)

LEE ET AL.

Examiner

Thuan N. Du

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 February 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Applicant is hereby requested to update the status of all copending applications indicated in the instant application.
2. Claims 1-17 are presented for examination.

Claim Objections

3. Claims 1-11, 14 and 15 are objected to because of the following informalities:

Claim 1 is objected because "the clock delay" in line 3 has not mentioned before.

Applicant is suggested to rewrite the phrase to -- a clock delay --.

Claims 2-5 are also objected for incorporating the above deficiency by dependency.

Claim 6 is objected because "the clock delay" in line 7 has not mentioned before.

Applicant is suggested to rewrite the phrase to -- a clock delay --.

Claim 8 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 8 recites the round trip delay time of the clock signal is estimated which is the same as the delay time of the clock signal is estimated based on the round trip travel time of said clock signal as recited in claim 6.

Claim 9 is objected because "a primary clock path" recited in claim 9 is the same as "a primary clock path" recited in claim 6. Therefore, the phrase "a primary clock path" recited in claim 9 should be rewritten as -- the primary clock path --.

Claims 7, 10 and 11 are also objected for incorporating the above deficiency by dependency.

Claim 14 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 14 recites the round trip delay time of the clock signal is estimated which is the same as the delay time of the clock signal is estimated based on the round trip travel time of said clock signal as recited in claim 12.

Claim 15 is objected because "a primary clock path" recited in claim 15 is the same as "a primary clock path" recited in claim 12. Therefore, the phrase "a primary clock path" recited in claim 15 should be rewritten as -- the primary clock path --

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 14 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 14 recites the limitation "said estimating step" in line 1. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 15 is also rejected for incorporating the above deficiency by dependency.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-3, 5-9, 11-15 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaplinsky (U.S. Patent No. 5,298,866).

10. **Regarding claim 1**, Kaplinsky teaches a method for distributing a clock signal generated by a clock generator (the clock generator which generates the CLOCK signal shown in Fig. 1) to a plurality of nodes on an integrated circuit [col. 1, lines 6-9] comprising the steps of:

estimating a clock delay for each of said nodes [col. 2, lines 66-67; col. 5, lines 27-28], wherein said clock delay includes clock generator output delays (fanout) [col. 1, line 62 to col. 2, line 2] and resistive-capacitive (RC) delays [col. 2, lines 8-18]; and

adjusting said clock signal for each node based on said estimated clock delay such that said clock signal arrives at each of said nodes with an aligned phase [col. 2, line 66 to col. 3, line 2; col. 6, line 53 to col. 7, line 2].

11. **Regarding claim 2**, Kaplinsky teaches the estimating step further comprises the step of estimating a round trip delay time for the clock signals [col. 3, lines 14-16].

12. **Regarding claim 3**, Kaplinsky teaches that the round trip delay time is obtained using a primary clock path (outward path 15) and a return clock path (return path 29) [Fig. 1; col. 3, lines 17-27; col. 5, lines 29-41].

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13. **Regarding claim 5**, Kaplinsky teaches the integrated circuit is a printed circuit board [col. 1, lines 12-16].

14. **Regarding claim 6**, Kaplinsky teaches a method for distributing a clock signal generated by a clock generator (the clock generator which generates the CLOCK signal shown in Fig. 1) to a plurality of nodes on an integrated circuit [col. 1, lines 6-9] comprising the steps of:

providing a feedback clock path for each of said nodes (path 29) [Fig. 1; col. 4, lines 46-49; col. 5, line 29], each of said feedback clock paths having an associated primary clock path that distributes said clock to each node (outward path 15) [Fig. 1; col. 4, lines 50-52; col. 5, lines 29-41];

determining a round trip travel time of said clock signal on each of said primary clock paths and associated feedback clock path [col. 3, lines 14-27];

estimating a clock delay for each of said nodes [col. 2, lines 66-67; col. 5, lines 27-28] using said round trip travel time [col. 3, lines 14-18; col. 5, line 29]; and

adjusting said clock signal for each node based on said estimated clock delay such that said clock signal arrives at each of said nodes with an aligned phase [col. 2, line 66 to col. 3, line 2; col. 6, line 50 to col. 7, line 2].

15. **Regarding claim 7**, Kaplinsky teaches that the clock delay includes a clock generator output delays (fanout) [col. 1, line 62 to col. 2, line 2] and a resistive-capacitive (RC) delays [col. 2, lines 8-18].

16. **Regarding claim 8**, Kaplinsky teaches the estimating step further comprises the step of estimating a round trip delay time for the clock signals [col. 3, lines 14-16].

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17. **Regarding claim 9**, Kaplinsky teaches that the round trip delay time is obtained using a primary clock path (outward path 15) and a return clock path (return path 29) [Fig. 1; col. 3, lines 17-27; col. 5, lines 29-41].

18. **Regarding claim 11**, Kaplinsky teaches the integrated circuit is a printed circuit board [col. 1, lines 12-16].

19. **Regarding claim 12**, Kaplinsky teaches a network for distributing a clock signal generated by a clock generator (the clock generator which generates the CLOCK signal shown in Fig. 1) to a plurality of nodes on an integrated circuit [col. 1, lines 6-9] comprising:

a primary clock path that distributes said clock to each node (outward path 15) [Fig. 1; col. 4, lines 46-52];

a feedback clock path associated with each said primary clock paths (return path 29) [Fig. 1; col. 5, lines 29-41];

a phase comparator (phase comparator 63) for determining a round trip travel time of said clock signal on each of said primary clock paths and associated feedback clock path [col. 3, lines 14-16, 28-29; col. 6, lines 43-45]; and

a delay driver (delay element 47 and /or 49) for adjusting said clock signal for each of said nodes based on an estimated clock delay for each of said nodes (small, large or the same) based on said round trip travel time [col. 2, lines 66-68; col. 3, lines 14-16; col. 6, line 50 to col. 7, line 2], such that said clock signal arrives at each of said nodes with an aligned phase [col. 2, line 66 to col. 3, line 2].

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20. **Regarding claim 13**, Kaplinsky teaches that the clock delay includes a clock generator output delays (fanout) [col. 1, line 62 to col. 2, line 2] and a resistive-capacitive (RC) delays [col. 2, lines 8-18].

21. **Regarding claim 14**, Kaplinsky teaches the estimating step further comprises the step of estimating a round trip delay time for the clock signals [col. 3, lines 14-16].

22. **Regarding claim 15**, Kaplinsky teaches that the round trip delay time is obtained using a primary clock path (outward path 15) and a return clock path (return path 29) [Fig. 1; col. 3, lines 17-27; col. 5, lines 29-41].

23. **Regarding claim 17**, Kaplinsky teaches the integrated circuit is a printed circuit board [col. 1, lines 12-16].

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

25. Claims 4, 10 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaplinsky (U.S. Patent No. 5,298,866).

26. **Regarding claims 4, 10 and 16**, Kaplinsky does not explicitly teach the integrated circuit is a system-on-chip. One of ordinary skill in the art would have readily recognized that it would have been obvious to apply the teaching of Kaplinsky to any environment, including system-on-chip, which uses clock distribution network for reducing clock skew [col. 2, lines 59-61].

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Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan N. Du whose telephone number is (703) 308-6292. The examiner can normally be reached on Monday-Friday: 9:00 AM - 5:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (703) 305-9717.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

The fax number for the organization is (703) 872-9306.



Thuan N. Du
January 21, 2004